OIPE JC25
APR 28 2005
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent Application of	)	
	)	
MIURA	)	**Art Unit 2186**
	)	
Application Number: 10/809,465	)	
	)	
Filed: March 26, 2004	)	
	)	
For: STORAGE CONTROLLER AND CONTROL METHOD OF THE SAME	)	
	)	
	)	
ATTORNEY DOCKET NO. ASAM.0117	)	

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

PETITION TO MAKE SPECIAL UNDER 37 C.F.R. § 1.102(d)

FOR ACCELERATED EXAMINATION

Sir:

Pursuant to 37 C.F.R. § 1.102(d), Applicant respectively requests that the application be examined on the merits in conjunction with the pre-examination search results, the detailed discussion of the relevance of the results and amendments as filed concurrently.

Substantive consideration of the claims is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and telephone number indicated below.

Respectfully submitted,

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STATEMENTS & PRE-EXAMINATION SEARCH REPORT SUPPLEMENTAL TO THE PETITION TO MAKE SPECIAL

Sir:

Pursuant to 37 C.F.R. §§ 1.102 and MPEP 708.02 VIII, Applicant hereby submits that (1) all claims of record are directed to a single invention, or if the Office determines that all the claims presented are not obviously directed to a single invention, will make an election without traverse as a prerequisite to the grant of special status; (2) a pre-examination search has been conducted according to the following field of search; (3) copies of each reference deemed most closely related to the subject matter encompassed by the claims are enclosed; and (4) a detailed discussion of the references pointing out how the claimed subject matter is patentable over the references is also enclosed herewith.

FIELD OF THE SEARCH

The field of search includes the following classes:

Class	Subclasses	Description
710/ DATA		**ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: INPUT/OUTPUT**
	1	INPUT/OUTPUT DATA PROCESSING

	5	. Input/Output command process
	8	. Peripheral configuration
	13	.. By detachable memory

Class	Subclasses	Description Continued)
713/		**ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: SUPPORT**
	200	SECURITY

The above subclasses represent areas deemed to contain subject matter of interest to one or more of the search features. The integrity of the search is based on the records as presented to us by the United States Patent and Trademark Office (USPTO). Also a key word search was performed on the USPTO full-text database including published U.S. patent applications.

The search was directed towards claims 1-13 of U.S. Application 10/809,465. The claims are generally characterized by a storage controller for receiving a data input/output request from an information processor and reading or writing data from or in a hard disk drive in accordance with the data input/output request, comprising: a circuit board provided with a nonvolatile memory functioning as a cache memory for storing the data to be read from or written in the hard disk drive; and a circuit board setting portion to which the circuit board is removably set; wherein the circuit board is provided with a removal information output circuit for outputting circuit-board removal information showing that the circuit board is removed from the circuit board setting portion and a data erase circuit for erasing the data stored in the nonvolatile memory when the circuit board removal information is output from the removal information output circuit. (See Conclusion paragraph for detailed references to drawings and specification).

LIST OF RELEVANT REFERENCES

The search revealed the following U.S. patents, which are listed for convenience:

U.S. Patent No.	Inventor
5,552,776	Wade et al.
5,935,244	Swamy et al.
6,289,397 B1	Tsuyuguchi et al.

U.S. Patent Application Publication No.	Inventor
2004/0143688 A1	Sugimoto

Discussion of References:

U.S. Patent No. 5,552,776 to **Wade** et al. was assigned to Z-Microsystems and entitled "Enhanced Security System for Computing Devices". **Wade**'s removable data storage modules 1303, 1305 (Fig. 13) of a security system for controlling access to computing devices (Abstract) each contains nonvolatile memory which may be configured on a printed circuit board (col. 5, lines 11-12, 35-38). Disks 1153, 1155, 1157 are accessed via an array controller 1158 (Fig. 11; col. 16, lines 54-55). The array controller 1158 communicates with a data storage bus 1151, which is connected to a data storage bus I/O port to other computing devices 1149. Selective access control is made possible incorporating non-volatile memory I/O ports inside both of the removable storage modules 1303, 1305 and a docking base unit 1300 (col. 16, lines 58-65). Counters integrated into the removable modules 1303, 1305 or affixed within the base unit 1300 may be available to indicate the number of insertions of the removable modules 1303, 1305 into the base unit 1300 and/or the number of times a disk drive within the removable modules 1303, 1305 is powered up or down (col. 21, lines 51-55). An electronic counter circuit can be provided with non-volatile memory for storing the number of times the removable modules 1303, 1305 are inserted and/or removed from the base unit 1300 (col. 21, lines 59-63). However, **Wade** only applies nonvolatile memory in the removable data storage modules 1303, 1305 and the electronic counter circuit, rather than in any cache memory. Neither the removable data storage modules 1303, 1305 nor the electronic counter circuit functions as a cache memory. As such, **Wade** does not provide "a circuit board provided with a nonvolatile memory functioning as a cache memory for storing the data to be read from or written in the hard disk drive" as recited in claims 1, 7 and 13. In addition, **Wade** does not provide on the same circuit any "removal information output circuit for outputting circuit-board removal information showing that the circuit board is removed from the circuit board setting portion" or any "data erase circuit for erasing the data stored in the nonvolatile memory when the circuit board removal information is output from the removal information output circuit" as recited in claims 1, 7 and 13.

U.S. Patent No. 5,935,244 to **Swamy** et al. was assigned to Dell USA, L.P. and entitled "Detachable I/O Device for Computer Data Security". **Swamy**'s system includes a personal computer 100 (Fig. 1; abstract) with a processor and a detachable I/O device 102

that functions as a conventional computer interface when docked to the computer 100. A "device present" pin is included in the detachable I/O device's 102 connector 106 to detect when the detachable I/O device 102 is connected to or detached from the computer 100 (col. 3, lines 33-36). A basic input output memory 524 is connected to a local bus 520. A FLASH memory or other nonvolatile memory is used as the BIOS memory 524 (Fig. 2; col. 4, lines 14-16). An I/O controller 575 is connected to an expansion bus 560. The I/O controller 575 is interfaced to both a hard drive 580 and a floppy diskette drive 585 (col. 4, lines 55-58). However, **Swamy** only applies the FLASH memory or other nonvolatile memory as the BIOS memory 524 of the personal computer 100 rather than in any cache memory. **Swamy** simply does not involve other hard drives than the IDE hard drive 580 (col. 4, line 57) to form any disk array 300, or any cache memory in a storage controller 100 for controlling a disk array. As such, **Swamy** does not provide any storage controller 100 with "a circuit board provided with a nonvolatile memory functioning as a cache memory for storing the data to be read from or written in the hard disk drive" as recited in claims 1, 7 and 13. In addition, **Swamy** does not provide on the same circuit any "removal information output circuit for outputting circuit-board removal information showing that the circuit board is removed from the circuit board setting portion" or any "data erase circuit for erasing the data stored in the nonvolatile memory when the circuit board removal information is output from the removal information output circuit" as recited in claims 1, 7 and 13.

U.S. Patent No. 6,289,397 B1 to **Tsuyuguchi** et al. was assigned to TEAC Corporation and entitled "Disk Drive or Like Peripheral Storage Device Adapted for Firmware Upgrading, Self-Testing, etc." **Tsuyuguchi**'s electrically erasable, programmable ROM (EEPROM) 44 (Fig. 2) in a USB interface 29 (Fig. 1) is employed for firmware storage. Each new firmware version is issued in the form of a flexible magnetic disk which may be loaded in a floppy disk drive (FDD) 5 like an ordinary data disk, *only with disk drive 5 disconnected from computer 1 as far as data transmission is concerned.* The EEPROM 14 is preprogrammed to identify the loaded firmware disk, to erase the old firmware version on the ROM, and to write the new version on the disk. A USB cable 2 has a connector 2a coupled to a connector 1a on the computer 1 and another connector 2b to a USB hub 3 (Fig. 1). A USB cable 4 has a connector 4a coupled to the USB hub 3 and a connector 4b to an FDD 5 (col. 4, lines 17-21). The FDD 5 includes an interface section 7 which may take the form of an interface board, having an FDD controller 28, the USB interface 29, and a supply circuit 30 mounted on a printed circuit board. The USB interface 29 is connected via a line 33

to a connector 31 to which a detachably coupled noted connector 4b on one end of the USB cable 4 leading to the USB hub 3 (col. 5, lines 31-37). The USB interface 29 comprises an input/output circuit 42 connected to the serial transmission signal line 33, a central processor unit 43, and the electrically rewritable nonvolatile memory or EEPROM 44 (col. 6, lines 8-13). The program in EEPROM 44 location 50 contains a startup subroutine for FDD 5 and another subroutine for rewriting or upgrading the firmware in EEPROM location 49 (col. 6, lines 29-32). The computer 1 is questioned at S7 whether the FDD 5 is ready for reading and writing. The FDD 5 includes means for determining whether or not the FDD 5 is electrically connected to the computer 1, and means for replacing an old firmware version on the EEPROM 44 with a new version on the firmware storage medium when the FDD 5 is determined to be not connected to the computer 1 (col. 2, lines 40-45, 52-55; col. 7, lines 52-55). However, **Tsuyuguchi** only applies the EEPROM 44 in the USB interface 29 of an FDD 5 rather than in any cache memory. **Tsuyuguchi** simply does not involve other FDDs to form any disk array 300, or any cache memory in a storage controller 100 for controlling a disk array. As such, **Tsuyuguchi** does not provide any storage controller 100 with "a circuit board provided with a nonvolatile memory functioning as a cache memory for storing the data to be read from or written in the hard disk drive" as recited in claims 1, 7 and 13. In addition, **Tsuyuguchi** does not provide on the same circuit any "removal information output circuit for outputting circuit-board removal information showing that the circuit board is removed from the circuit board setting portion" or any "data erase circuit for erasing the data stored in the nonvolatile memory when the circuit board removal information is output from the removal information output circuit" as recited in claims 1, 7 and 13.

U.S. Patent App. Pub. No. 2004/0143688 A1 of **Sugimoto** was assigned to Hitachi, Ltd. and entitled "Storage Device Controlling Apparatus and a Circuit Board for the Same". **Sugimoto**'s storage device controlling apparatus 100 (Fig. 1; [0010]) is coupled to a storage device 300 for storing data and coupled to an information processing apparatus 200 via a network 400. An integrally unitized circuit board 118 (Fig. 8) can be attached to the storage device controlling apparatus 100. An input-output controller 114 (Fig. 7; [0099]) sends and receives data and command to and from a disk controllers 140 (Fig. 10; [0142]), a cache memory 130, a shared memory 120, and a managing terminal 160. The input-output controller 114 comprises I/O processors 119 and the NVRAM 115. The NVRAM 115 stores a program to control the I/O processors 119. The disk controller 140 (Fig. 10) includes an NVRAM 144 is a nonvolatile memory storing a program to control the CPU 142. The

contents of a program stored in the NVRAM 144 can be written or rewritten according to instructions from the managing terminal 160 or the NAS manager 706 described later ([0102], [0105]). However, **Sugimoto** only applies the NVRAM 115 in the input-output controller 114 and the NVRAM 144 in the disk controller 140 (Fig. 1), rather than in the cache memory 130. As such, **Sugimoto** does not provide "a circuit board provided with a nonvolatile memory functioning as a cache memory for storing the data to be read from or written in the hard disk drive" as recited in claims 1, 7 and 13. In addition, **Sugimoto** does not provide on the same circuit any "removal information output circuit for outputting circuit-board removal information showing that the circuit board is removed from the circuit board setting portion" or any "data erase circuit for erasing the data stored in the nonvolatile memory when the circuit board removal information is output from the removal information output circuit" as recited in claims 1, 7 and 13.

Conclusion

Based on the results of the comprehensive prior art search as discussed above, Applicants contend that the storage controller as now recited in independent claims 1, 7 and 13, especially the features of "a circuit board provided with a nonvolatile memory functioning as a cache memory for storing the data to be read from or written in the hard disk drive," or any "removal information output circuit for outputting circuit-board removal information showing that the circuit board is removed from the circuit board setting portion" and any "data erase circuit for erasing the data stored in the nonvolatile memory when the circuit board removal information is output from the removal information output circuit" on the same circuit are patentably distinct from the cited prior art references.

In particular, as now recited in the claim 1 (for example, the embodiment shown in Figs. 1, 9-10; pp. 24-25, and 29-31), the storage controller 100 for receiving a data input/output request from an information processor 200 and reading or writing data from or in a hard disk drive 300 in accordance with the data input/output request, comprising: a circuit board 130 provided with a nonvolatile memory 131 functioning as a *cache memory* for storing the data to be read from or written in the hard disk drive 300; and a circuit board setting portion 180 (Fig. 3; p. 16, line 26 to p. 17, line 3) to which the circuit board 130 is removably set. The circuit board 130 is provided with a removal information output circuit 135 for outputting circuit-board removal information showing that the circuit board 130 is

removed from the circuit board setting portion 180, and a data erase circuit 133 for erasing the data stored in the nonvolatile memory 131 when the circuit board removal information is output from the removal information output circuit 135.

The invention recited in claim 7 is directed to a method for controlling the storage controller 100 recited in claim 1.

The invention recited in claim 13 is directed to a storage controller including a first circuit board on which a channel control portion 110 for receiving a data input/output request from an information processor 200 and outputting an I/O request corresponding to the data input/output request is formed; a second circuit board on which a shared memory 120 in which the I/O request is stored is formed; a third circuit board on which a disk control portion 140 for reading or writing data from or in a hard disk drive in accordance with the I/O request stored in the shared memory is formed; the circuit board setting portion 180 and the circuit board 130 as recited in claim 1.

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art references, Applicant respectfully contends that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable consideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and telephone number indicated below.

Respectfully submitted,

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